FPGA based control systems for space instrumentation: examples from the IAPS experience

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Abstract. INAF IAPS research groups have a long time expertise in the production of scientific instrumentation for space missions. Thanks to ASI funding and in collaboration with the national industries leader in the space sector, IAPS, the Institute for Space Astrophysics and Planetology of INAF, often participates in the development of control electronics for space instrumentation. Over the years, the need to use FPGAs for the implementation of some of the instrument control functionalities (microcontrollers, interfaces, algorithms data processing) has increased, thanks to their small size and weight, very low power consumption, radiation tolerance and high reliability. This contribution provides a brief description of some examples of IAPS developed systems, highlighting what may be the potential need for future collaborations.

Key words. Space instrumentation - FPGA - instrument control

1. Introduction

In the past decade Italy has gained a leading role in the production of control electronics for scientific payloads onboard astronomical space missions and the involved Italian industries acquired an expertise that today allows them to compete at the same level of all the other major European companies. Analogously, within the European Consortia of research institutes responsible for the scientific instruments provision, the Italian research institutes can today be considered as the reference partners for the production of the payload control electronics hardware and software.

This leading role is clearly confirmed by looking at the long list of missions in which Italian institutions, and in particular the Institute for Space Astrophysics and Planetology (IAPS) of the Italian National Institute for Astrophysics (INAF), have been involved in the past or are presently contributing in the development phase. These contributions are listed in Table 1 where missions with an Italian research institute participation at proposal level have been included as well, to provide a complete picture of the potentialities for these activities. The list in Table 1 should not be considered as exhaustive of all Italian contributions to space missions, but has the scope to provide a figure of the Italian involvement in the design and development of payload scientific instruments control electronics.

Looking more in detail to the table, it can be seen that INAF IAPS can today be considered as a reference institute in this field. In most cases the provided electronics (both HW and SW) is the result of a partnership be-
Table 1. Main Astronomical and Planetological Space missions with an Italian responsibility in the instrument control HW/SW.

<table>
<thead>
<tr>
<th>Mission #</th>
<th>Instrument</th>
<th>HW contribution</th>
<th>SW contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESA Infrared Space Observatory (ISO)</td>
<td>Long Wavelength Spectrometer</td>
<td>Instrument control and data handling electronics (Laben S.p.A.)</td>
<td>Instrument control and data acquisition SW (CNR IFSI)</td>
</tr>
<tr>
<td>ESA Mars Express Mission</td>
<td>PFS</td>
<td>Instrument control and data handling electronics (CNR IFIS)</td>
<td>Instrument control and data acquisition SW (CNR IFSI)</td>
</tr>
<tr>
<td>ESA Venus Express Mission</td>
<td>PFS</td>
<td>Instrument control and data handling electronics (CNR IFIS)</td>
<td>Instrument control and data acquisition SW (CNR IFSI)</td>
</tr>
<tr>
<td>ESA Herschel mission</td>
<td>All three focal plane instruments (PACS, SPIRE, HIFI)</td>
<td>Instrument control and data handling electronics (CGS S.p.A.)</td>
<td>Instrument control and data acquisition SW (CNR IFSI)</td>
</tr>
<tr>
<td>ESA Planck Mission</td>
<td>LFI</td>
<td>Instrument control and data handling electronics (Thales Aixen Space M. ex Laben)</td>
<td>Instrument control and data acquisition SW (CNR IASF and Laben)</td>
</tr>
<tr>
<td>NASA JUNO mission</td>
<td>JIRAM</td>
<td>Instrument control and data handling electronics (SElex-ES)</td>
<td>Instrument control and data acquisition SW (IAPS and SElex-ES)</td>
</tr>
<tr>
<td>NASA DAWN mission</td>
<td>VIR</td>
<td>Instrument control and data handling electronics (SElex-ES)</td>
<td>Instrument control and data acquisition SW (IAPS and SElex-ES)</td>
</tr>
<tr>
<td>ESA Bept Colombo missions</td>
<td>SERENA</td>
<td>Instrument control and data handling electronics (CGS, AMID, and IAPS)</td>
<td>Instrument control and data acquisition SW (CGS, AMID, and IAPS)</td>
</tr>
<tr>
<td>ESA ExoMars mission</td>
<td>MAMISS</td>
<td>Instrument control and data handling electronics (Leonardo Finmeccanica)</td>
<td>Instrument control and data acquisition SW (Leonardo Finmeccanica and IAPS)</td>
</tr>
<tr>
<td>ESA Euclid Mission</td>
<td>All two (VIS and NISP) payload instruments</td>
<td>Instrument control and data handling electronics (CGS S.p.A.)</td>
<td>Instrument control, data acquisition and compression SW (INAF IAPS, IAES, OAIO, OAEP)</td>
</tr>
<tr>
<td>ESA Plato Mission</td>
<td>Payload computer</td>
<td>Instrument control and data handling electronics (Italian industry to be selected)</td>
<td>Instrument control and data acquisition SW (INAF IAPS)</td>
</tr>
<tr>
<td>ESA Athena Mission</td>
<td>IFU</td>
<td>Instrument control and data handling electronics (Italian industry to be selected)</td>
<td>Instrument control, data acquisition and compression SW (INAF IAPS, IAES, OAIO, OAEP)</td>
</tr>
<tr>
<td>ESA ECHO mission proposal</td>
<td>Payload 5 bands spectrometer</td>
<td>Instrument control and data handling electronics (INAF OAA and Italian industry)</td>
<td>Instrument control and data acquisition SW (INAF IAPS)</td>
</tr>
<tr>
<td>ESA Ariel mission Proposal mission proposal</td>
<td>Payload instruments</td>
<td>Instrument control and data handling electronics (INAF OAA and Italian industry)</td>
<td>Instrument control and data acquisition SW (INAF IAPS)</td>
</tr>
<tr>
<td>JAXA-ESA SPICA mission Proposal</td>
<td>SAFARI Spectrometer</td>
<td>Instrument control and data handling electronics (INAF OAA and Italian industry)</td>
<td>Instrument control, data acquisition and compression SW (INAF IAPS)</td>
</tr>
<tr>
<td>ESA Phoenx mission proposal</td>
<td>All two payload instruments chassis</td>
<td>Instrument control and data handling electronics</td>
<td>Instrument control, data acquisition and compression SW (INAF IAPS)</td>
</tr>
<tr>
<td>NASA Europa Clipper Mission proposal</td>
<td>MUSE</td>
<td>Instrument control and data handling electronics</td>
<td>Instrument control, data acquisition and compression SW (INAF IAPS)</td>
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between an Italian industry and the research institute. This results is a direct consequence of the policy adopted by ASI, the Italian Space Agency, whose funding strategy is based on the need to strengthen the Italian aerospace industry presence in the international arena. In this type of collaboration, IAPS plays a vital role in two phases of the project: i) the initial phase of definition of the requirements and the high level architecture of the instrument control electronics, with the consequent production, when possible, of a feasibility study, and ii) the final stage of acceptance and testing of the final product.

For this type of activity a multipurpose prototyping and testing framework is being developed at IAPS, with the aim of characterizing the usage of the most promising space qualified processors and interfaces. The framework has been designed based on the analysis
of the main functionalities of a generic instrument control unit for a space instrument, i.e. an instrument that shall operate autonomously for most of the time, being commanded using time tagged commands uploaded in a timeline updated only once per day. The needed functionalities, therefore, are: - Telemetry (TM) and Telecommand (TC) exchange with the spacecraft (S/C); - Instrument Commanding, based on the received and interpreted TCs - Instrument monitoring and control, based on the Housekeeping data (HK) acquired from the other instrument components; - Detectors readout data acquisition, pre-processing (including onboard lossless or lossy compression) and formatting according to the selected Telemetry protocol; - Synchronization of all the instrument activities.

To implement the above described functionalities, a set of (semi-)standard requirements on the instrument control electronics can be derived and a generic architecture can be designed. In the past, the standard electronics architectures (e.g. ISO, Herschel, Planck missions, see Table 1) included different custom boards to implement i) the instrument control functions in a CPU board hosting the processor and the memories, ii) the interface with the subsystems of the instruments and iii) the interface with the spacecraft. This concept has evolved with time into a more structured approach, where multipurpose boards are adopted, with the aim of minimizing the mass and power consumption budgets and the overall costs.

In particular, for the system prototyping in the feasibility study phase a FPGA based design can be adopted. FPGAs are in general suitable devices to meet the requirements that characterize the instrument control systems onboard space instrumentation: small size and weight, very low power consumption, radiation tolerance and high reliability. Moreover, the FPGA reconfigurability is a desirable feature during a study phase, because it allows to easily try and evaluate different processor
solutions, which can also be complemented with the required peripherals and data communication interfaces. The present contribution is focused on the presentation of some of the elements presently working in the framework, based on the use of FPGAs to implement part of the needed functionalities. In particular, in section 2 the adopted FPGA based CPU prototype board is presented, with a short introduction to the LEON processor, one of the most promising new generation processors for space applications and in section 3 the developed low-level SpaceWire link analyser is described. In section 4 the test environment used to validate the framework elements is shortly described. In addition, IAPS is involved in many planetary exploration missions which involve also the need to design and develop miniaturised instrumentation (both sensors and electronics) to be used onboard rovers or landers. In section 5 a description of the FPGA based instrument control system prototyped for the MIMA experiment, a spectrometer designed for the ExoMars rover, is provided.

2. The CPU breadboard

In the IAPS prototyping environment, the fault-tolerant LEON processor system has been selected as the main processor. LEON is a 32-bit SPARC-compliant processor (see section 3), which results from ESA’s efforts in the development of processors for space applications (see http://microelectronics.esa.int/components/comppage.htm). It has already been used in several space missions (e.g. the Swedish PRISMA mission, the European Space Agency Proba-2, GAIA and BepiColombo) and it is planned to be used also in a number of medium size missions competing in the frame of the ESA Cosmic Vision program.

The size of the breadboard developed for the prototyping activities (see Di Giorgio, A. M. et al. 2010) is compatible with the possibility to include a LEON processor, a SpaceWire (see ECSS 2008) routing switch, all the required memory chips, and an auxiliary FPGA. An additional processor dedicated to the data compression functionality could be added if necessary (see the considerations reported at the end of this section). A high level block diagram of the board architecture is shown in Figure 1 while a picture of it is shown in Figure 2. The LEON SoC is assumed to have three SpaceWire link (see ECSS 2008) interfaces, but a fourth interface is required in case cross strapping to the Satellite Command and Data Management System (CDMS) is to be implemented.

A detailed list of the technical characteristics of the breadboard is given in Table 1. The board includes a medium-size capacity FPGA from Xilinx (XC3S1500), which enables the implementation of complex designs. The breadboard have been used to assess the feasibility of the proposed design for the Instrument control unit of the European instrument SAFARI onboard the proposed M5 ESA-JAXA SPICA mission.

The amount of memory available on board (16 MB SRAM + 8 MB Flash) can be extended via a memory expansion connector. Furthermore, a mezzanine slot allows expansion to a coprocessor board, which can perform processing functions such as data compression algorithms.

A commercial non radiation tolerant Xilinx Spartan3 FPGA has been chosen for this breadboard as it is a low cost solution suitable for our architectural evaluation purposes. FPGA development has been fully supported by a series of free software tools included in the Xilinx ISE WebPackTM Design Suite, which offers a complete design flow (synthesis, place&route, device programming, simulation).
Table 2. Technical details of the CPU board

<table>
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<tr>
<th>Component #</th>
<th>characteristics</th>
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| FPGA        | – Xilinx Spartan-3 FPGA XC3S1500 (1.5Mgates) in a 456-pin BGA package  
– Xilinx Flash Proms for storage of FPGA configuration: XCF04S (4 Mbit) and XCF01S (1 Mbit) |
| Memory      | – SRAM: 16 MB (4M x 32)  
– NOR Flash: 8 MB (configurable as 8M x 8 or 4M x 16)  
– Memory Expansion Connector (120 pin) (e.g. for addition of SDRAM modules) |
| Interfaces  | – 3 SpaceWire Connectors for LVDS signals from the XC3S1500 FPGA  
– 1 SpaceWire Connector for LVDS signals from the Coprocessor Mezzanine Board  
– JTAG connectors for both Parallel Cable III and Parallel Cable IV |
| Board       | – USB Connector to provide a RS232 link (through a USB-to-UART bridge controller)  
– JTAG connectors for both Parallel Cable III and Parallel Cable IV |
| Expandability | – Slot for the Coprocessor Mezzanine Board (two 20x3 pin female header connectors) |
| User IO     | – Header connectors for user I/O signals: up to 16 signals from the XC3S1500 FPGA and up to 16 signals from the Coprocessor Board  
– LEDs, DIP Switch and Push Buttons for user-definable functions |
| On Board    | – 3.3V (I/O voltage), 2.5V (auxiliary voltage), 1.2V (core voltage) obtained from a single 5V power supply |
| Power Regulators | – 50 MHz oscillator  
– optional user-fitted oscillator |
| Board size  | – 114 x 60 mm |

3. SpaceWire link analyser

The network implemented in the prototyping framework is a SpaceWire network. SpaceWire is a standard (see ECSS 2008) for high speed networks on-board space missions developed by the University of Dundee with support from the European Space Agency (ESA).

It uses serial full-duplex links with the speed up to 200Mbits/sec to connect distributed equipments both at spacecraft level and within payload instruments. In such SpaceWire networks both application data and control information are transmitted at the same time. In particular, at instrument level, the need of synchronising the data acquisition with the commanding of movements of mechanical/optical parts (e.g. gratings, shutters, mirrors etc.) is the main cause of very stringent timing requirements on the network transactions. The IAPS framework, therefore, includes a low-level link analyzer (see Liu S. T. et al. 2014) to monitor bidirectional data in SpaceWire links in a non-intrusive way and to characterize the network timing performances. The developed FPGA based analyzer have simplified the network traffic analysis activity and provided a
useful tool for the integration and test phases in the development of space instrumentation.

With respect to the standard traffic analyzers, the developed one collects signals coming from pod probes connected in-series on the interested links. This solution allows to avoid the use of very long cables and the introduction of undesired delays. In addition, the tool design includes the possibility to internally reshape the LVDS signal, increasing the robustness of the analyzer towards environmental noise effects and guaranteeing a deterministic delay on all analyzed signals. Data are collected synchronously, a common time reference is used to tag information and a time reference generator feeds the same timing information to each decoding sub-unit, thus guaranteeing a coherent time-tagging with the minimal jitter (see Sheynin Y. et al. 2007) for each event. The analyzer core is implemented on a Xilinx Spartan6-LX45 FPGA. Three main logical entities have been designed to perform decoding, re-grouping and signal buffering, and a USB link is used to relay the collected information to a computer for analysis (see Figure 3). The analyzer performances have been tested both in terms of decoding capabilities and in terms of induced time jitters and delays. The traffic analyzer allowed the characterisation of the synchronisation capabilities of the IAPS framework SpaceWire network. The intrinsic analyzer properties, with a maximum induced delay on the measured signals of less than 10ns and a negligible additional jitter, allowed to measure the intrinsic time jitter introduced by the adopted router transmitters in the time codes (see Parkes, S. 2003) propagation in two different regimes, with and without concurrent data traffic.

4. Framework elements testing environment

To test the developed BreadBoard and to familiarize with the LEON processor and the communication over SpaceWire, we set-
up a dedicated testing environment in which three framework elements have been included and tested: the CPU BreadBoard, a commercial development board (GR-XC3S-1500, a product by Gaisler Research and Pender Electronic Design), and a custom mezzanine board plugged into the BreadBoard. Each of the boards in the test set-up carries a processor and these processors have been connected to form a SpaceWire network.

This network is intended to mimic the connection between the SpaceCraft (S/C), the instrument, and a coprocessor. The LEON3 SoC on the BreadBoard has the role of the instrument CPU, while the same SoC on the GR-XC3S-1500 board has been used to simulate the S/C command and data management unit. For the coprocessor, a 16-bit microcontroller (C16, [http://www.opencores.com/projects.cgi/web/c16/overview](http://www.opencores.com/projects.cgi/web/c16/overview)) has been implemented on the mezzanine board. SpaceWire routers have been included into the various FPGA designs to provide the processors with multiple connection ports. To perform the tests, dedicated application codes have been written in C for the various processors, using the RTEMS operating system. A simple protocol has been devised on top of SpaceWire to enable the exchange of messages between the nodes of the network. Using this protocol, the S/C simulator node can send requests of data packets to the CPU Breadboard node or its coprocessor, which can reply accordingly. The test execution can be driven and monitored from a host PC connected through a RS232 link to the S/C simulator node.

5. The experiment MIMA onboard ExoMars

Another example of the IAPS involvement in the design and development of FPGA based instrument control electronics refers to a planetary exploration mission: MIMA (micro-Martian Infra-red Mapper), a Fourier Spectrometer operating in the infrared for the ESA mission ExoMars 2016. To be mounted on a descending module to Mars, it was designed to observe the Martian atmosphere after landing and to study the features of the atmosphere gas-composition (analysis of methane presence in particular) to make conclusions
about possible biological activity and to check
the meteorological conditions at the landing
site. Being an instrument to be mounted on
a rover, it was subject to severe design con-
straints: limited mass, size and power budget,
high stress resistance for the landing shock,
severe environmental conditions without any
power for thermal control, resistance to the
strong vibrations of the high acceleration lev-
els in wide frequency range. IFSI (now IAPS)
designed and prototyped the instrument con-
trol unit, whose functions were to read, store
and transmit in telemetry the acquired science
and housekeeping data, to control the spec-
trometer movement and to initiate/terminate a
measure (spectral acquisition). The unit pro-
totype was synthesized on a Xilinx XC3S400
FPGA using the Memec Spartan-3 LC devel-
opment board. With reference to the unit
was composed by two microcontrollers. The
main microcontroller, based on the C16 model
running at 25MHz, implemented the spectra
acquisition and the communication protocol
with the rover. The secondary microcontroller
(KCPSM3 picoBlaze3) was used to control the
total displacement and velocity (implementing
the Proportional Integral and Derivative algo-
rithm) of the spectrometer mirrors. In figure the
realised miniaturised board is shown. It im-
plements all the instrument control and data ac-
quision/processing functionalities necessary
to the experiment and has a size of less than
100mm x 100mm. Unfortunately, due to a de-
scoping of the ExoMars rover hosting capabil-
ities (in terms of allowed mass and volume)
the MIMA experiment has been cancelled. The
IAPS acquired expertise in miniaturised elect-
onelectronics is presently very useful for the prepara-
tion of competitive proposals for future planetary
exploration missions.

6. Conclusions
Given the increasing involvement of the INAF
research institutes in space missions, the acqui-
sition of a specific expertise focused on the use
of FPGAa (both ASICs and reprogrammable
FPGAs) in space is necessary. In this contrib-
ution some examples of the IAPS experience
in using FPGA devices for the prototyping and
testing activities of control systems for space
instrumentation have been provided. The use of
one of the most promising european fault
tolerant processors (LEON) onboard an FPGA
based breadboard has been described as well as
the development of a traffic analyser to be used
on Spacewire networks (ECSS-E-ST-50-12C), used
in many of the most recent ESA and JAXA
missions. Finally the high level description of
a miniaturised control electronics prototyped
for the ExoMars MIMA experiment has been
provided, as an example of the IAPS expertise
in designing fault tolerant applications based
on microcontrollers developed for commercial
scopes.

References
ECSS-E-ST-50-12C, 2008 European Cooperation for Space standardization (ECSS), SpaceWire: Links, nodes, routers
and networks