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R&D experiences on FPGAs and astronomical applications at IASF Milano

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Abstract. The paper describes R&D activities that were or are currently developed at the INAF - IASF Milano and that involve the usage of FPGAs for astrophysical applications. They span from the emulation of radiation induced faults in SRAM-based FPGAs to the development of a backend unit for the SKA low frequency antennas and astronomical detectors.

Key words. FPGA – Front-end electronics – fault emulation – Astronomical applications

1. Introduction

Field Programmable Gate Array (FPGA) devices are widely used in many today's applications, favored by their attractive characteristics, namely high gate density, performances, flexibility, and reduced development costs.

The ones based on SRAM technology (SRAM-FPGA) are known to be susceptible to radiation induced single event effects that might affect the behavior of implemented circuits when used in space applications. The predominant radiation effect in this kind of devices is the Single Event Upset (SEU). Suitable countermeasures to ensure correct operation in space are required, (e.g. Triple Modular Redundancy - TMR, configuration memory scrubbing) and the resulting SEU sensitivity of designs implemented in SRAM-FPGAs must be assessed.

The paper presents R&D activities that were or are currently developed at the INAF - IASF Milano and that involve the usage of FPGAs for astrophysical applications. They span from the emulation of radiation induced faults in SRAM-based FPGAs to the development of a backend unit for the SKA low frequency antennas and astronomical detectors.

2. FLIPPER

FLIPPER was a project funded by the European Space Agency that spanned over ten years, starting in 2004 and yielding two major system releases (Alderighi at al. 2007). The project objective was the development of a fault emulation platform for SRAM-based FPGA devices aimed at the evaluation of the effects of radiation induced faults, and in particular the effects of single svent upsets. SEUs are of particular concern for SRAM-FPGAs, because they affect not only flip-flops and RAM blocks of the user design, but also the device configuration memory, they can therefore change the logical function of the circuit.

In FLIPPER, SEUs are emulated by fault injection into the configuration memory, onto which a design can be mapped. The fault model adopted in FLIPPER is the bit-flip of configuration memory cells. This is accom-

Fig. 1. FLIPPER Hardware platform. The picture shows the control board and the DUT board with a Xilinx XC4VSX55 stacked on it.

plished by frame modification and active partial re-configuration. Locations of the configuration memory cells to alter are randomly determined.

FLIPPER consists of a hardware platform and a software application running on a PC. The hardware platform includes a flexible FPGA-based general purpose board (control board) that can be employed in other SEU testing activities (namely, ground radiation test), and also in more general applications as a testbed equipment or a digital I/O board. There is also a daughter board, stacked on the control board, hosting the Device Under Test (DUT board). In the first release of the system, the control board hosted a Virtex-II Pro device (XC2VP20) and the DUT device was a Qpro Virtex-II device (XQR2V6000); in the second release the FPGA device in the control board is a Virtex-5 device (XC5V FX70), while the DUT board hosts a Virtex-4 device (XC4VSX55).

As compared to its predecessor, the current release also features a 1Gbit/s Ethernet link toward the PC, replacing the old USB channel, and 1 DDR2 SODIMM in place of the old onboard chip. A picture of the current FLIPPER hardware platform is shown in Fig. 1. Test stimuli and reference (gold) output vectors for the functional test of the design are imported by the software application from a test-bench simulated in a VHDL/Verilog simulator. The software includes features to import test/gold vectors in Extended Value Change Dump format (EVCD, IEEE Standard 1364-2001).

FLIPPER allows for a quantitative characterization of design robustness and comparison of design hardening techniques, as well as tuning of design redundancy and protection. Several experimental activities were accomplished by the FLIPPER platform (e.g. Alderighi et al. 2008, Liu et al. 2011, Liu et al. 2012). The fault model was experimentally validated through proton radiation testing experiments at the TSL (Theodor Svedberg Laboratory, Uppsala, Sweden) facility in 2007 (Alderighi et al. 2009) and at the PSI (Paul Sherrer Institute, Villigen, Switzerland) facility in 2008 (Alderighi et al. 2010).

FLIPPER was developed in collaboration with Sanitas EG company.

3. Highly reliable COTS based computing sytem - Hi-Rel CoCs

In 2008 the European Space Agency launched three programs aimed at using COTS components for the development of space computers, able to provide either high reliability (Hi-Rel program), high performance (Hi-P program) or high availability (Hi-V program).

In the context of the Hi-Rel program, the development of a high reliability on board computer, based on COTS technology, was undertaken (Hi-Rel CoCs project). The project team was composed by Thales Alenia Space Italia (Prime Contractor), Politecnico di Torino, University of Rome Tor Vergata, Sanitas EG srl company, and INAF. The INAF was responsible for: the technological survey of candidate reprogrammable logic devices, the definition of the evaluation environment and test campaigns, and the design and implementation of the Electrical Ground Support Equipment (EGSE) for the Hi-Rel CoCs computer.

The main features of the computing system are as follow:

- a CPU based on PowerPC (PPC)7448;
- a working memory based on a double data rate II (DDR II) memory;
- a high speed SRAM-based FPGA (a Xilinx Virtex-4 device) for implementing the bridge toward memory, and other high-functionalities;
- a scrubber unit for the Virtex-4 FPGA, to correct Single Event Upsets in the configuration memory;
- a combination of software and hardware Fault Detection, Isolation and Recovery (FDIR) strategies. The hardware features specifically supporting software FDIR are the following:
  - selective memory protection;
  - individual memory power switching to cope with Single Event Functional Interrupt (SEFI);
  - smart watch-dog (supervisor) to check program flow.
- the following ESA standard data interfaces
  - SpaceWire;
  - High Speed Serial links.

The Hi-Rel CoCs project, which concluded in December 2014, resulted in a highly reliable space computer that is also able to provide high computing performance. Project results were described in Esposito et al. 2015.

4. TPM board for SKA low frequency antennas

The Tile Processing Module (TPM) is a data acquisition and processing board for the Low Frequency Aperture Array (LFAA) antennas of the SKA radio telescope. The project is included within the activities of the SKA Aperture Array Design and Construction, for the Signal Processing task, which are in charge of the Oxford University.

The project has been developed thanks to a funding program of the INAF, TECNO INAF 2012, (title "Digital Platform development for back end design of new generation SKA Aperture Arrays", National coordinator INAF - Catania Astrophysical Observatory), and has been supported by industrial partners, such as Xilinx and Analog Devices, as technology suppliers.

The project is actually a co-funding initiative of INAF (namely, Catania Astrophysical Observatory, Arcetri Astrophysical Observatory, Institute for Radioastronomy, Institute for Space Astrophysics and Cosmic Physcs - IASF Milano), Oxford University, Malta University, Science and Technology Facilities Council, and Sanitas EG company.

The scientific challenges that SKA has to face will imply technological challenges regarding the realization site. LFAA antennas

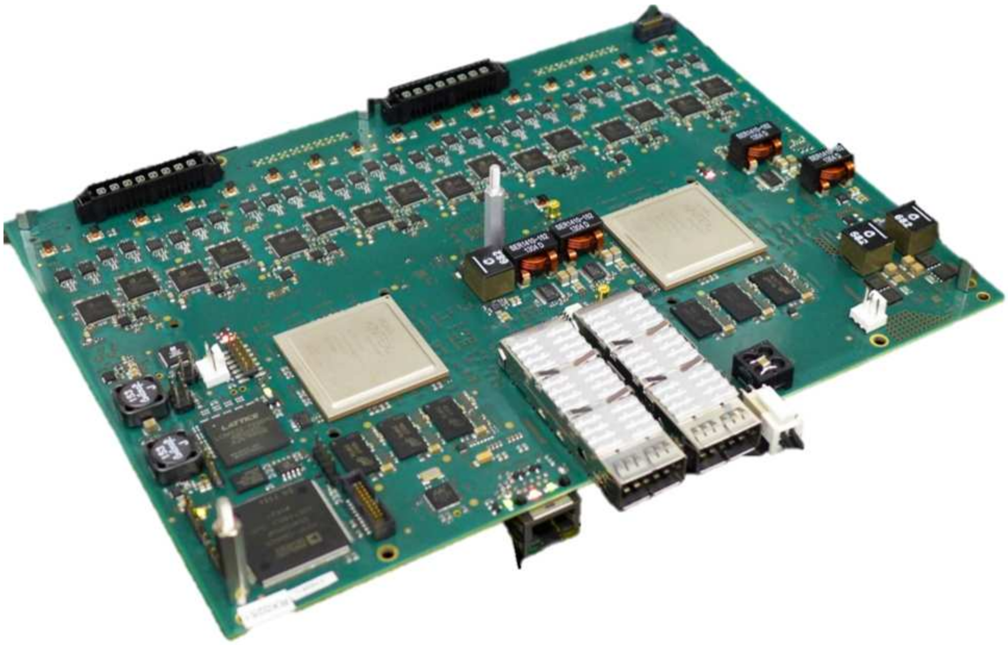

Fig. 2. TPM hardware platform for SKA LFAA.

that will be installed in South Africa and Australia at the end of Phase 1 construction will be about 131,000, spread on a wide desert land. Some of the technological challenges are the on-line processing of large amounts of data, the availability of limited energetic resources, and transport and distribution of this large amount of data.

In order to satisfy the processing requisites for the SKA LFAA antennas, no commercial technological solutions are actually available on the market; thus, the design and implementation of dedicated and ad hoc systems is necessary. The board prototype that has been manufactured is a modular element of a system that will consist in up of 10,000 modules, organized in a hierarchical fashion. The board acquires, digitizes, and processes signals coming from a set of antennas of the radio telescope, and in particular, in our case the set is made up 16 antennas. The board features novel characteristics and can be described as follows: i) an analog part, performing high frequency acquisition and conversion of analog signals coming from the antennas; ii) a digital part, accomplishing high performance filtering and preprocessing of acquired data. The main characteristics of the board, pictured in Fig. 2 , are the following:

- 32 analog inputs (16 antennas in double polarization) with ADC sampling up to 1 Gsample/s;
- High speed internal bus for high performance data processing (400 MHz internal bus);
- Result communication on high speed digital channels (80 Gbit/s);
- Massive data elaboration by using cutting edge Xilinx Ultrascale FPGA devices (20nm);
- High integration density;
- Low power solution.

The first TPM prototype was released on mid-January 2015.

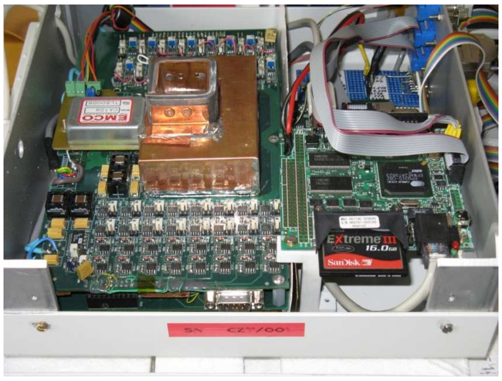

Fig. 3. The SIDERALE payload. In the foreground on the left, the ADC board stacked on the FPGA-based board, the pre-amp shield, and the detector assembly (16 pixels CZT) on top of it; on the right, the single board computer and the 16 MB Flash memory.

5. SIDERALE

SIDERALE (Alderighi et al. 2010a) was an experiment hosted as a piggy back payload on SoRa LDB (Sounding Radar Long Distance Balloon) mission by the Italian Space Agency (ASI). It was aimed at testing a detector for high energy astrophysics applications based on a 4x4 pixel CZT solid state sensor.

The electronics mainly included three subsystems: i) the analog unit, which performs pulse shape acquisition of the CZT signals (including charge amplifiers, buffers and trigger generation), ii)the digital unit, iii) and the power unit (Fig. 3).

The digital unit consists of an FPGA-based board and a single board computer. The FPGA-based board is a FLIPPER board (Alderighi et al. 2007) using a Xilinx Virtex-II Pro (XC2VP20) device. The interface towards the analog unit is made by the two 240-pin connectors. The board hosts 128 MByte of either SDRAM or DDR memory and 16 MByte Flash.

6. Photon counting intensified CCDs and APS

Photon counting detectors based on micro-channel plates (MCP) are the most used in a number of applications in UV/EUV astronomy and solar physics, since no other technology, up to now, can provide the same combination of large format (both in terms of sensitive area and number of pixels), photon counting capability, virtually null readout noise, possibility of optimizing the detector for different wavelength ranges with appropriate choice of the photocathode (with solar blindness option, with very high rejection of the visible light, characteristics very appealing for astronomical applications, since astronomical sources are typically orders of magnitudes brighter in the visible than in the UV), radiation hardness and operation at room temperature.

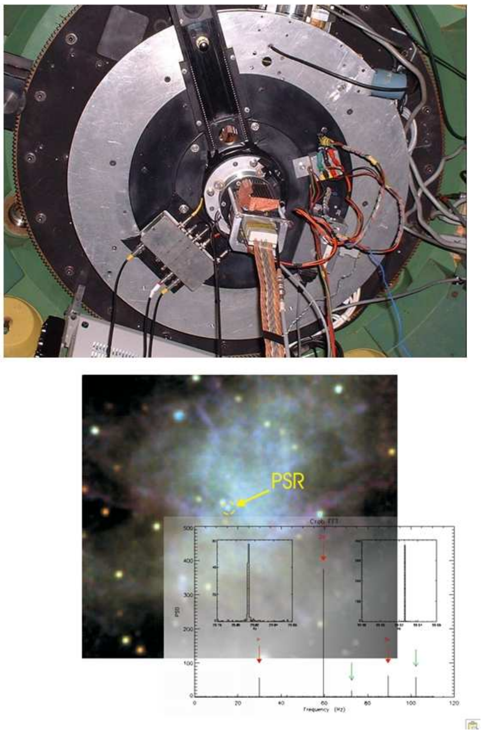

Fig. 4. The PC-ICCD mounted at the 182 cm cima Ekar telescope. Below: observation of the Crab nebula and fourier analysis of the photons from the Crab pulsar.

An R&D program on MCP-based detectors, readout by means of silicon image sensors, has been carried out at IASF-Milano since the ‘90s, originally funded by a specific ASI

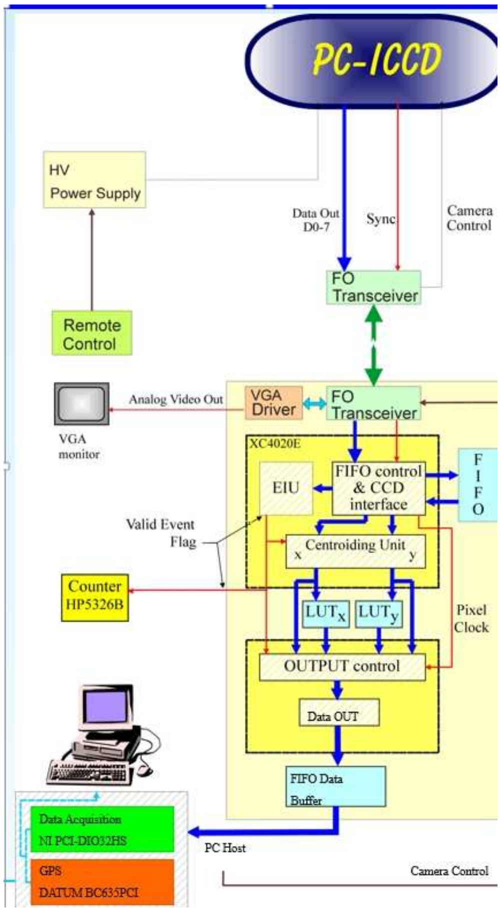

Fig. 5. Block diagram of the ICCD optimized for the optical range.

contract and then continued as support activity for mission concept studies, both for UV astronomy (UVISS - Scuderi et al. 2000, WSO - Pace et al. 2009) and solar physics (ASCE - Romoli et al. 2003, Solar Orbiter - Antonucci et al. 2012). Prototypes of detectors readout with CCD and APS have been realized, in which photon events, generating an electron cascade through a high gain MCP stack, are transduced, via a phosphor screen and a fiber optics reducer, into a quasi-Gaussian charge distributions on a CCD or APS matrix.

The sensor is readout at the highest frame rate and its output data flow shall be processed in real time by a digital processing electronics able to search for the presence of photon event footprint, satisfying a give set of morphological rules. For each event detected, the centroid coordinates are then computed with sub-pixel accuracy, and subsequently stored as photon list of coordinates.

One key component of these systems is the real time digital processing electronics which shall not limit the dynamic range of the system and must be able to sustain a very high data rate. A real time processing unit implemented in FPGA (originally implemented in Xilinx XC4013, Bergamini et al., 2000) can fulfill the requirements and can be easily adapted to different sensors (prototypes have been built, based on Xilinx XCV800, to process up to 500 Mpixel/s data rate - Bonanno et al. 2001, Uslenghi et al. 2001, Uslenghi et al. 2003).

6.1. Photon counting ICCD for visible range observations

A Photon Counting Intensified CCD optimized for the optical range has been realized in 1998 (Uslenghi et al. 2000) and used at the Catania 91 cm and Asiago 182 cm telescopes for high time resolution photometry and spectroscopy (in combination with AFOSC, the Asiago Faint Object Spectrograph and Camera) of Cataclysmic Variables and flare stars (see Fig.4). The core of the real time image processor has been implemented using FPGA Xilinx XC4020E. After several upgrades (Uslenghi et al. 2004), the detector is still working: the block diagram of the current configuration is shown in Fig.5.

7. Solar Orbiter/METIS UVDA detector

Specific studies aimed to optimize photon counting intensified detectors for solar physics applications, with particular emphasis on operations in harsh radiation environment, have been carried out with PRIN MIUR funding (2007) and then applied to the framework of the Solar Orbiter M1 ESA mission for the METIS (Multi Element Telescope for Imaging and Spectroscopy) instrument (Uslenghi et al. 2012). Solar Orbiter will be launched in October 2018 and its objective is the explo-

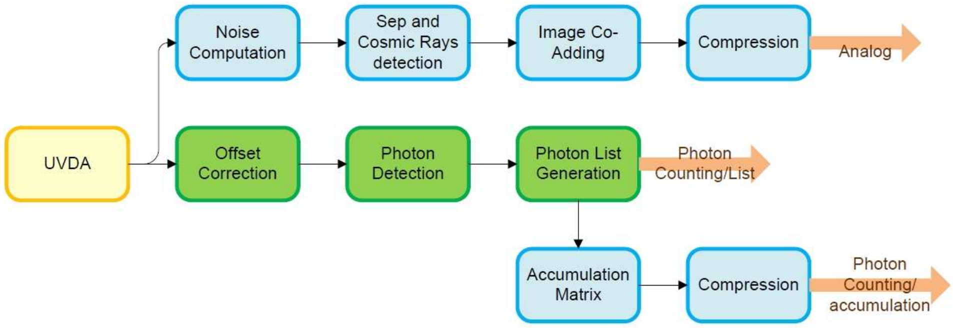

Fig. 6. Block diagram of the UVDA on-board processing. The green box have been implemented in the IP core PCU, along with the UV flux monitoring flags.

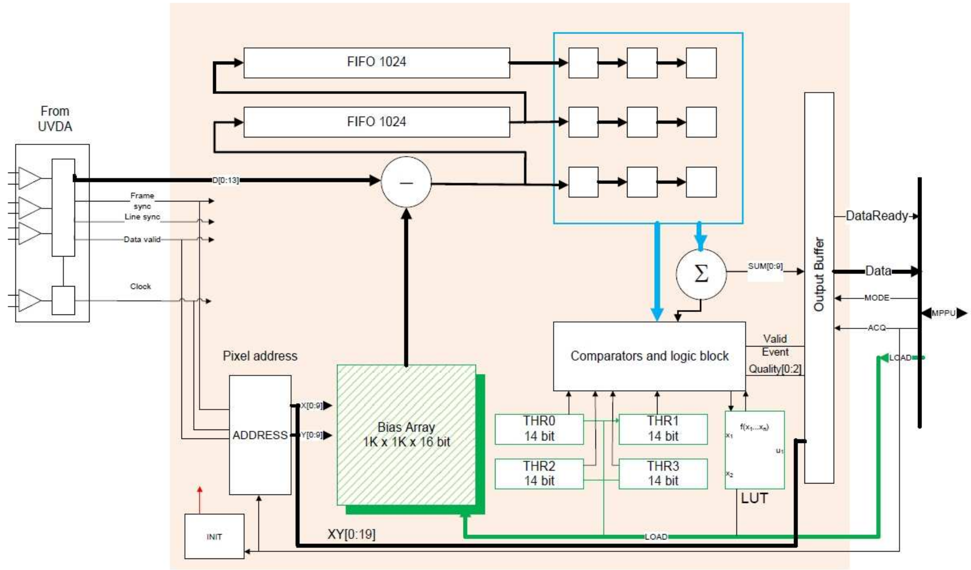

Fig. 7. Block diagram of the PCU IP core.

ration of the Sun-heliosphere connection, with a combination of remote sensing and in-situ instruments, from a distance that will reach 0.28 AU and from solar latitudes that will reach up to 34°.

METIS is one of the remote sensing instruments, an inverted-occultation coronagraph that will image the solar corona in two different wavelengths (visible light between 590 nm and 650 nm, and the Lyman-a lines of the hydrogen at 121.6 nm) by a combination of multilayer coatings and spectral bandpass filters. METIS has two detectors, one (VLDA, Visible Light Detector Assembly) is CMOS APS for the visible band and one (UVDA, Ultraviolet Detector Assembly) Instensified CMOS APS for the UV channel. For the UVDA an IP core (PCU, Photon Counting Unit) for Actel RTAX FPGA has been developed, with Sanitas EG srl, implementing the photon counting algorithms for the APS frame data processing and the UV flux monitoring flags to avoid over-

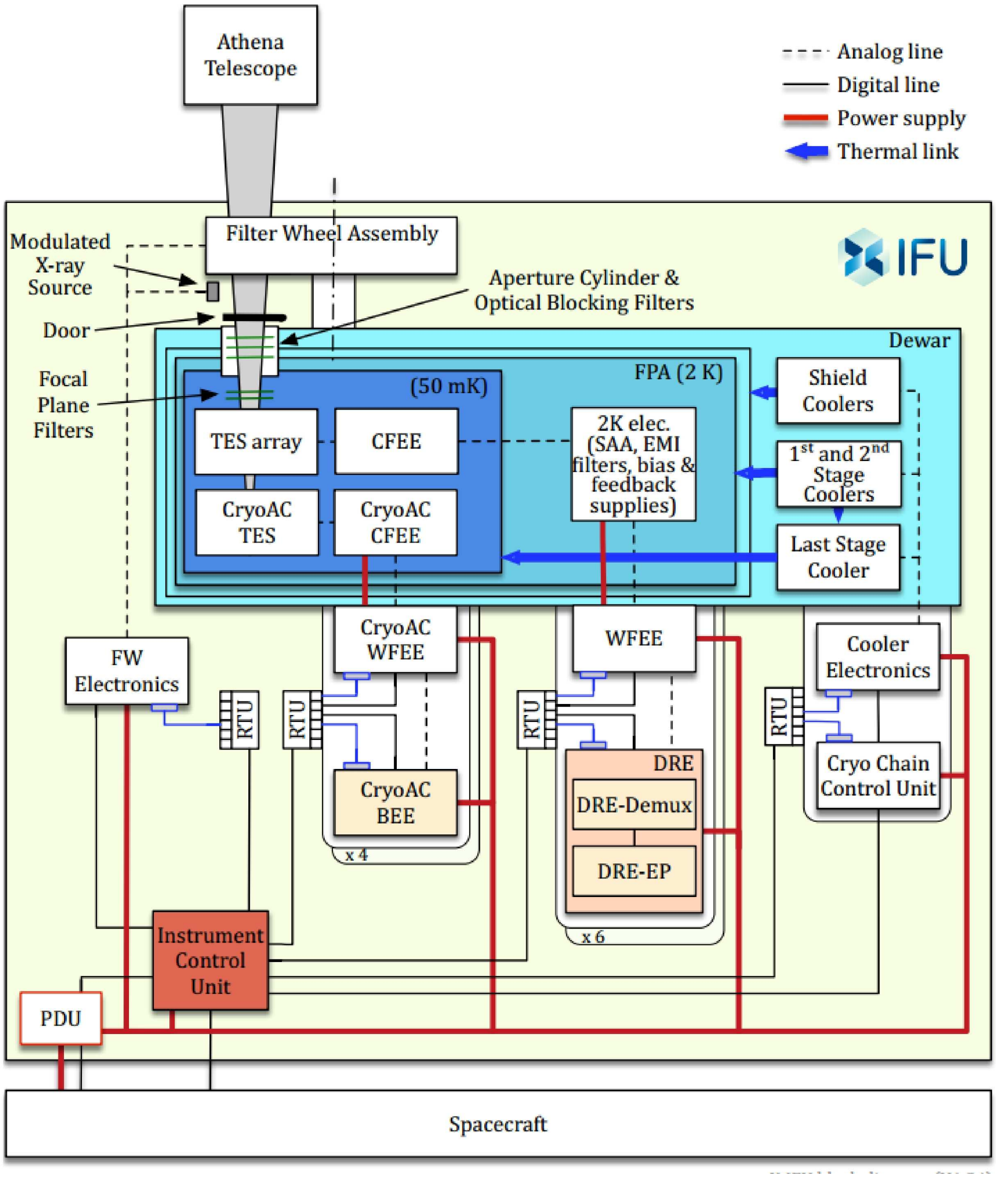

Fig. 8. Block diagram of the ATHENA XIFU.

illumination of the detector in case the sun disk appears in the FoV. The diagram of the UVDA on-board processing is shown in Fig.6, the green boxes have implemented in the PCU IP core (Fig.7).

8. General purpose CCD controller and data acquisition system

An R&D program, funded by INAF with a Tecno-PRIN 2009, has been carried out

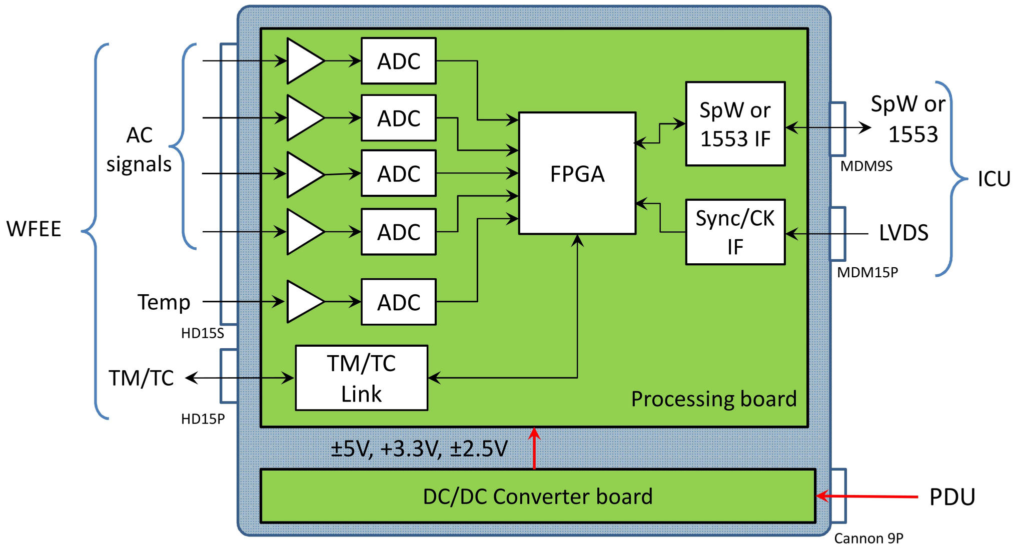

Fig. 9. Block diagram of the WBEE.

to develop low noise Front End Electronics implemented in ASIC (Application-Specific Integrated Circuit) for reading Charge Coupled Devices (CCDs) with highly segmented architectures and multiple parallel outputs (Schembari et al. 2014). The primary target was the realization of a photon counting x-ray detectors with time resolution in the order of ms, still retaining the almost Fano-limited energy resolution achievable with sensors readout at low frequency. A testing system has been designed to test CCDs and their FEE ASICs. The main guideline has been to develop a general purpose system which could be used to test several different devices, optimizing the system for the particular pair Sensor/FEE by just changing one single board (the focal plane board).

The general purpose CCD controller, the ASIC sequencer and the data acquisition system have been implemented with standard National Instruments FPGA-based modules:

1. one FlexRIO 7952R with the digital adapter module NI 6581 (54 single-ended digital I/O channels, up to 100 MHz clock frequency), mainly implementing the ASIC sequencer and the CCD controller
2. one FlexRIO 7952R with the ADC adapter module NI 5761 (4 channels sampled at 14 bit, 500 MHz bandwidth and up to 250 MS/s sample rate), for the data acquisition.

The modules are hosted in a PXI chassis PXI-1042Q. The system is controlled by Labview software. Module 1 allows programming the internal register of the FEE ASIC via SPI interface and implements a controller with up to 32 signals to generate the phases of the CCD and the waveforms to control the FEE ASIC. The master clock is selectable up to 80 MHz allowing a time resolution of 25 ns in the definition of the waveforms. The maximum delay between the signals generated by the controller is less than 1 ns. A software interface has been developed in IDL (Interactive Data Language) to provide an user-friendly way to configure the sequencers. Module 2 allows real time processing of the digitized output waveform, applying digital filtering or more complex processing. The flexibility provided by the XILINX Virtex-5 FPGA hosted on the National Instruments board allows quick testing and optimization of the waveforms for different devices and of the output signal processing.

9. Future work: Athena XIFU CryoAC WBEE

ATHENA is the second large-class ESA mission, in the context of the Cosmic Vision 2015 - 2025, scheduled to be launched on 2028 at L2 orbit. One of the two on-board instruments is the X-IFU (X-ray Integral Field Unit, block diagram in Fig.8): a TES-based array able to perform simultaneous high-grade energy spectroscopy and imaging. The X-IFU sensitivity is degraded by the particles background induced by primary protons of both solar and Cosmic Rays origin, and secondary electrons. In order to reduce the background expected in L2 orbit to enable the characterization of faint or diffuse sources (e.g. WHIM or Galaxy outskirt), an active anticoincidence is required. Thus, a Cryogenic AntiCoincidence (CryoAC - Macculi et al. 2016), based on a 4-pixels detector made of wide area Silicon absorbers sensed by Ir TESes, will be placed at a distance less than 1 mm below the TES-array. The output signals of the CryoAC detector will be digitized by 4 ADCs at 100KHz and processed by an FPGA-based digital signal processor, hosted on the Warm Back End Electronics (Fig.9). The WBEE will implement:

– the pulse discrimination and detection system,
– the processing of the digitized waveforms in order to extract relevant physical parameters (time constants, amplitude, temporal distance from the previous event, . . .),
– the VETO signals generator (VETO LOGIC)
– the control logic.

All the main digital function will be implemented in a digital processing board based on FPGA.

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